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A 10 Gs/s latched comparator witch dynamic offset cancellation in 28 nm FD-SOI process

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ABSTRACT

This papers presents a high-speed, latched comparator implemented in industrial 28 nm FD-SOI technology. A novel approach to counter the mismatch is proposed. The solution employs trimming the threshold voltage by means of modulating of back-gate polarization of FD-SOI transistors. The comparator is a first step towards the design of a complete 4-bit FLASH analog-to-digital converter, with a sampling frequency of 10 GHz.

Keywords: FD-SOI, mismatch compensation, analog circuits, comparator, nanometer technology

1. INTRODUCTION

The Fully-Depleted Silicon-On-Insulator processes emerge recently as a successor of the traditional CMOS technology and compete with Fin-FET processes [1, 2, 3, 4]. The FD-SOI technology allows to produce ICs as fast as those realized in Fin-FET process but the FD-SOI chips consumes less energy.

The specific feature of the transistor manufactured in FD-SOI process (which utilizes ultra-thin buried oxide) is that the transistors can be treated as double-gate devices. The possibility to control polarization of the back-gate (Fig. 1) offers the IC designers a whole new spectrum of possible solution. A typical CMOS process design kit usually contains several NMOS/PMOS devices of different threshold voltages like: low-V_T, regular-V_T, high-V_T, etc. With introduction of FD-SOI back-gate biasing designer needs only two types of MOS transistors: low-V_T and regular-V_T since the other types can be obtained simply by changing the back-gate bias voltage. This FD-SOI feature can be exploited also in the analog domain. The most interesting one is compensation of the device mismatch, e.g. in the input stage of a comparator, by means of trimming the threshold voltage by means of modulating of back-gate polarization.

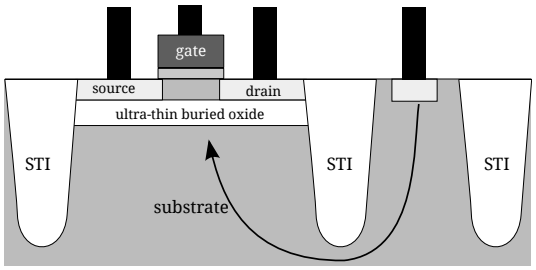

Figure 1. The cross-section of the transistor structure realized in FD-SOI process.

The design of latched comparator presented in this paper is the first steps towards the fast (10 GHz sampling frequency) FLASH analog-to-digital converter. This in turn is a part of project which aim is to implement the intelligent cyclic ADC [5] in the 28 nm FD-SOI process.

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2. THE COMPARATOR

2.1 The basic design

A voltage comparator is a widely used block. It usually appears in mixed-mode designs at the border of the digital domain and the analog world. The most typical area of application of such a generic component is the FLASH ADC where the most desirable feature is high speed. On the contrary, the high precision comparator is needed as an offset detector in a digitally controlled offset compensation circuits [6]. Wherever a comparator is utilized it significantly influence the design parameters, e.g. resolution and speed of the ADC or the effectiveness of the offset compensation [7].

When a comparator is used in a FLASH ADC it should be as fast as possible and have to present precision that is no worse then 1/2 LSB (least significant bit). However, these requirements are contradictory and usually one of the parameters has to be sacrificed in favor of the another. The presented design is high speed application oriented. Practically, the only feasible solution in such a case is so called latched comparator [8, 9, 10, 11]. The complete schematic of the design is presented in Fig. 2. The example simulation results of the comparator are shown in Fig. 3.

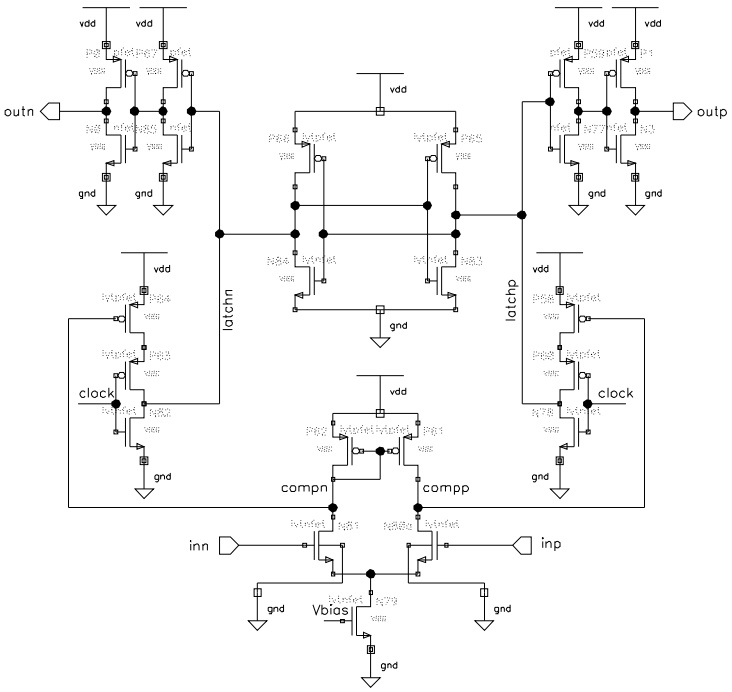

Figure 2. The basic design of the latched comparator. The back-gates of the input transistor pair are grounded.

The comparator consists of three stages: differential input amplifier, regenerative latch and two buffers that separate latch outputs from the load. The first stage constantly compares the input signals *inn* and *inp*. The two output voltages: *compn* and *compp* are fed to the dynamic inverters that drive (signal *latchn* and *latchp*) the output latch. When the *clock* signal is *low* the nodes labeled *latchn* and *latchp* are set to value resulting from the values of *compn* and *compp*. When *clock* changes to *high* state the new value is being stored in the latch. The buffers (built from transistor of the highest possible V_T) provide the clean comparison result. This result is valid until clock returns to *low* state.

In the case of the presented design, which will be utilized in a 4-bit ADC, the comparator resolution should be at least 30 mV. As can observed on the example plots (Fig. 3) this target has been reached. However, the resolution is comparable to the mismatch of the input pair transistors. Thus, a offset compensation solution must be applied otherwise the comparator is useless. The modification, however, must not degrade the sampling frequency what means it should be performed on the fly.

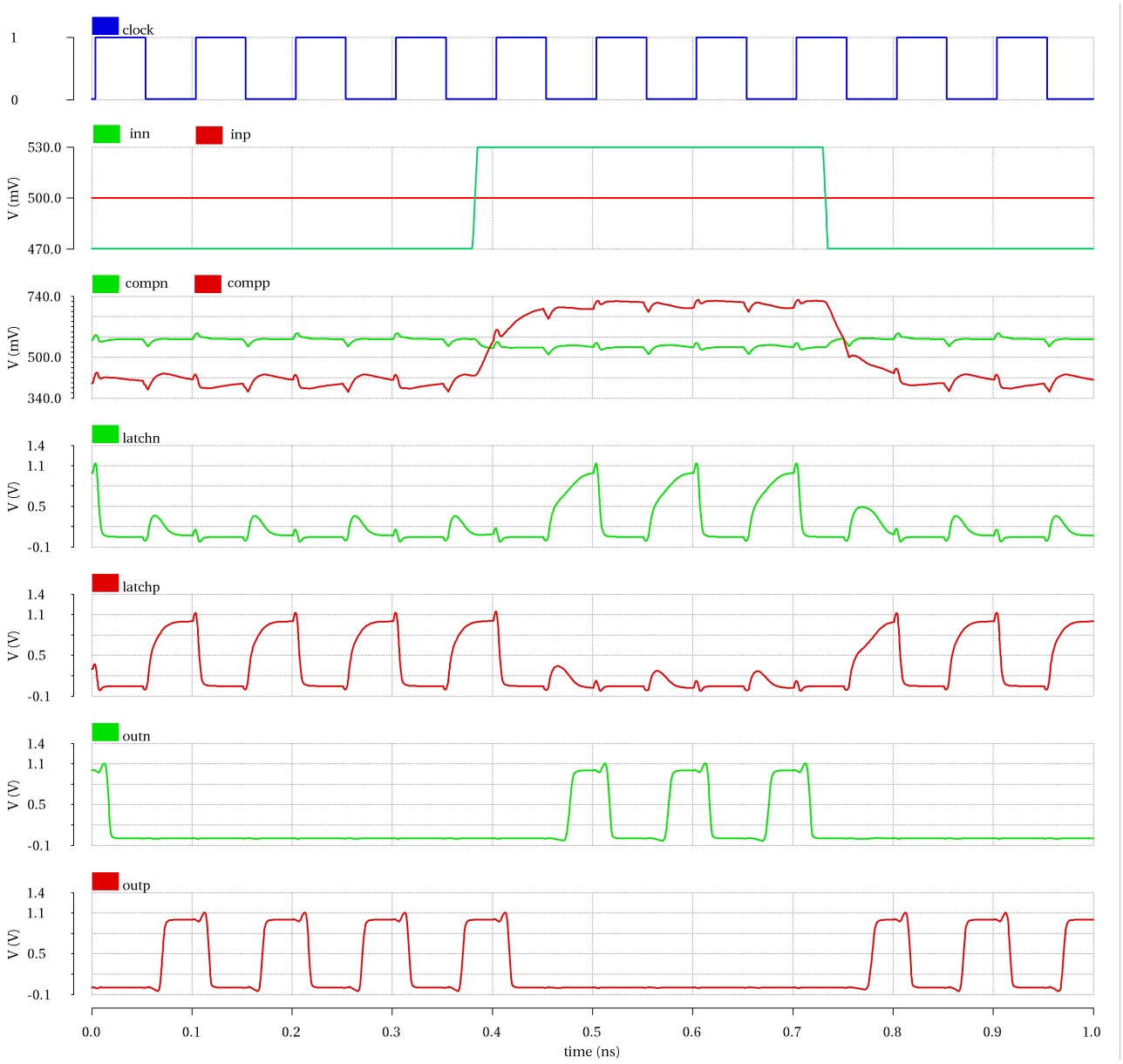

Figure 3. The results of transient simulation of the base (uncompensated) design.

2.2 Mismatch compensation

Over the years, several techniques have been developed to minimize circuit sensitivity to process variations [12, 13, 14, 6, 15, 16, 17]. These approaches can be divided into two groups: first related to the schematic design (e.g. chopping, auto-zeroing) and second dealing with the circuit layout (e.g. common-centroid transistor layout). In fact, design techniques from both these groups have to be applied in a design in order to counter the random and the deterministic process disturbances.

In case of FD-SOI technology the most suitable mismatch counter-measure seems to be trimming of transistor's threshold voltage by means of back-gate bias modulation [4]. The Fig. 4 presents dependency of a NMOS transistor $Id = f(V_{GS})$ characteristic on the back-gate polarization voltage.

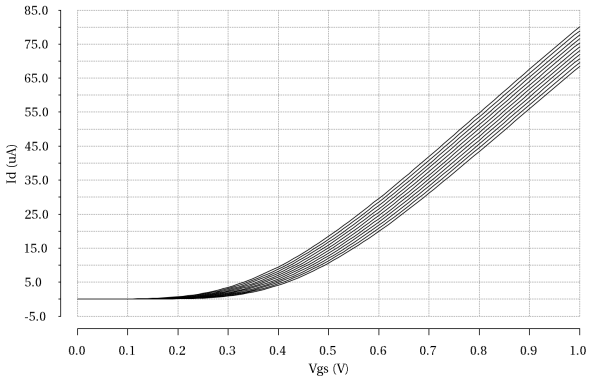

Figure 4. The NMOS transistor $Id = f(V_{GS})$ characteristic obtained for back-gate biasing in the 0...1 V range.

2.3 The comparator with offset cancellation

The comparator equipped with offset cancellation circuitry is shown in Fig. 5. It works interchangeably in two modes: comparing the inputs or mismatch compensation. When the *clock* signal is *low* the input amplifier senses the $V_{inn} - V_{inp}$ difference. When *clock* changes to *high* state the new output value is immediately stored in the latch and the design is reconfigured into offset cancellation mode.

The idea of the mismatch compensation is to short-circuit the gates of the input pair transistors and adjust the back-gate biasing. The bias voltages, V_{nbias} and V_{pbias}, are obtained by means of charging capacitors with the currents that are proportional to (amplified) $V_{compn} - V_{compp}$ difference. Due to leakage currents and switching noise the V_{nbias} and V_{pbias} voltages decay over time and have to be periodically restored.

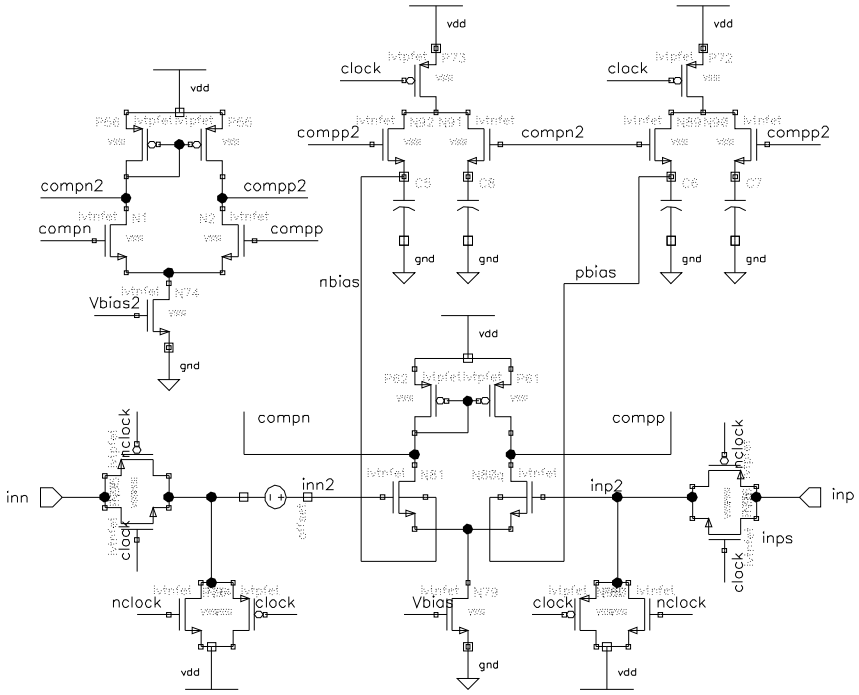

Figure 5. The comparator with mismatch compensation circuitry (the output latch and buffers are not shown here).

The plots presented in Fig. 6 show how the input offset (simulated with additional voltage source) influence the comparator without the mismatch compensation. The output is wrong. The second set of plots (Fig. 7)

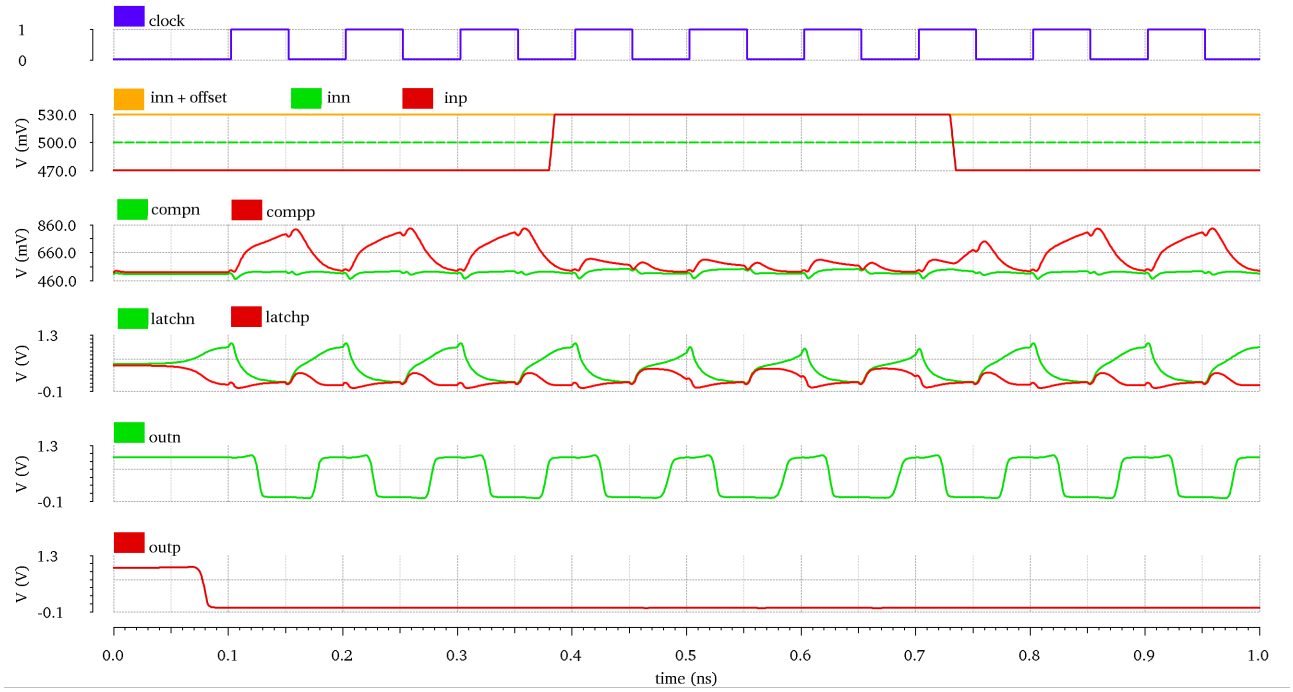

Figure 6. The results of simulation of the comparator without offset compensation – the output is wrong.

presents performance of the comparator with offset cancellation circuitry. In this case, the simulated offset of 30 mV is compensated by trimmed back-gate biasing and the comparator output is correct.

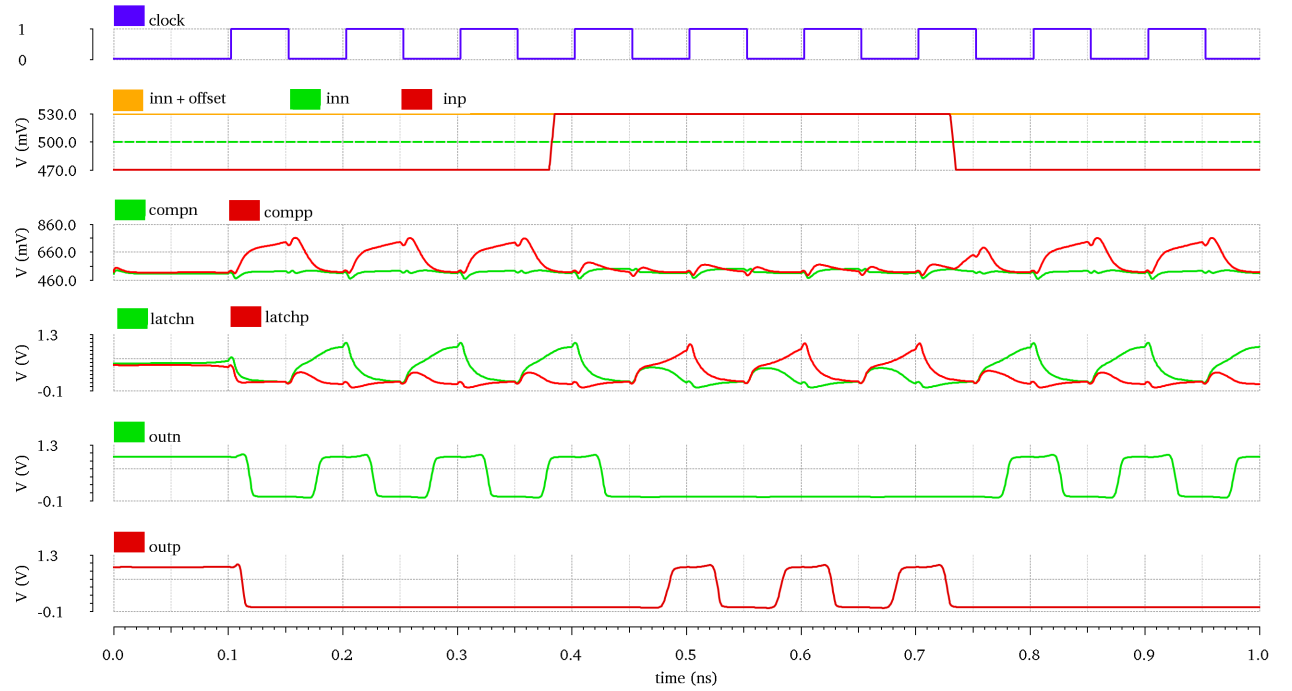

Figure 7. The results of simulation of the comparator with offset compensation – the output is correct.

3. CONCLUSIONS

The paper presents the design of latched comparator in the 28 nm FD-SOI technology, operating at 10 GHz frequency. The resolution of 30 mV makes the comparator suitable for application in 4-bit FLASH ADC. The novel approach to mismatch compensation, based on trimming of transistor's threshold voltage by back-gate bias modulation, guarantees that the design offset in kept at reasonable level.

4. ACKNOWLEDGMENTS

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